REMARKS/ARGUMENTS

35 USC § 112

The Office objected that the title is not sufficiently specific. The applicant has amended the title herein to "DEVICE OPERABLE AS NMOS OR PMOS".

The Office rejected claims 7 and 17 as being indefinite with respect to the "tolerance". The applicant agrees, and has amended those claims to reflect altered dependency. Claim 1 is now dependent upon 4, which recites a tolerance, and alternatively upon claims 5 or 6, which are themselves dependent upon claim 4.

The Office noted that there were two claims numbered "claim 15". This discrepancy is resolved herein by renumbering the first claim 15 as claim 21.

The Office rejected claim 17 (which is dependent upon claim 16) as failing to enable one of ordinary skill make the claimed inverted, logic gate, and memory cell from the circuit of claim 16. The applicant disagrees. An inverter using the technology is shown in Figures 4a, 4b, 4c, 4d (see spec. page 13, line 11 to page 14, line 15. A logic gate using the technology is shown in Figures 9a and 9b (see spec page 8, lines 19-22). Instructions for making a memory cell using the technology is included at spec. page 41, lines 7-10.

Double Patenting

The Office rejects claims 1-18. 11-17. 19 and 20 as non-statutory double patenting over US 6674099 to the same inventor. These rejections are resolved by concurrent filing of a terminal disclaimer.

35 US § 102

The Office rejected claim 18 as being unpatentable over Figures 3, 8 of Rao (US 4319263), and further over Figure 2a of EP 0 749 162. The applicant resolves those rejections by amending the claim to be dependent upon allowable claim 17.

The Office rejected claims 1, 2, 16, and 17 as being anticipated by Welch 5663584 or 6268636. Claim 1 and its dependencies are amended herein to recite that the device has sufficiently symmetric paths from source to drain for electrons and for holes such that the device

acts like a NMOS when drain to source (VDS) and gate to source (VGS) voltages are positive, and acts like a PMOS when drain to source (VDS) and gate to source (VDS) voltages are negative. Neither of the Welch references teach, suggest, or motivate one of ordinary skill in the art with respect to symmetric paths. Support is found in the pending spec. at page 7, lines 8-13.

Claim 16 and its dependencies are amended herein to recite that the device contains at least some Germanium. Neither of the Welch references teach, suggest, or motivate one of ordinary skill in the art to include Germanium in their Fig. 4b device (which is described as polycrystalline silicon). Support is found throughout the pending spec., e.g., at page 7, lines 14-17.

Request For Allowance

Claims 1-21 are pending in this application. The applicant requests allowance of all pending claims.

Respectfully submitted,
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